REMARKS

Claims 7-30 were pending in the present application. Claim 30 has been cancelled. Claims 7, 15-20, 22, and 30 have been amended. Accordingly, claims 7-29 are now pending in the application.

Claims 7-15 and 18-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Rowlands et al. (U.S. Patent No. 6,948,035) (hereinafter "Rowlands1") in view of Rowlands et al. (U.S. Patent Publication No. 2004/0034747) (hereinafter "Rowlands2"), and Chen et al. (U.S. Patent No. 6,931,496) (hereinafter "Chen"). Although Applicant respectfully traverses at least portions of the rejection, Applicant has amended the claims to expedite allowance.

Claims 16-17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Rowlands 1, Rowlands2, Chen and further in view of Hagersten et al. (U.S. Patent No. 5,940,860) (hereinafter "Hagersten"). Applicant respectfully traverses this rejection.

Applicant's claim 1 as amended, recites a multi-node system comprising in pertinent part

> "a node including a plurality of active devices and an interface coupled by an address network configured to convey address packets between the interface and the plurality of active devices, and a data network configured to convey data packets between the interface and the plurality of active devices, wherein the address network and the data network are separate networks;
> an inter-node network configured to convey coherency messages between the interface in the node and an additional interface in an additional node, wherein the additional interface is configured to send a coherency message requesting a read access right to a coherency unit on the inter-node network, wherein a given active device of the plurality of active devices has an ownership responsibility for the coherency unit;
> wherein the interface is configured to respond to the coherency message by sending a **proxy address packet** on the address network;
> wherein a different active device of the plurality of active devices is configured to request a read access right to another coherency unit by sending an address packet on the address network;

wherein the given active device of the plurality of active devices has an ownership responsibility for the another coherency unit, wherein the given active device is configured to not transition the ownership responsibility for the another coherency unit in response to the address packet and to transition the ownership responsibility for the coherency unit in response to the proxy address packet." (Emphasis added)

The Examiner asserts these features are taught by the combination of cited references. More particularly, the Examiner asserts Rowlands1 teaches the active devices coupled by the address and data networks in fig. 1, 12A-12N and col. 12, lines 19-25. Applicant respectfully disagrees. Specifically, Rowalnds 1 actually teaches at col. 12, lines 19-43

"Turning now to FIG. 3, a block diagram of one embodiment of a portion of the node 10 is shown in greater detail. In the embodiment of FIG. 3, the interconnect 22 may include a split transaction bus comprising an address bus 22A and a data bus 22B. Transactions may include an address phase transmitted on the address bus 22A and a data phase transmitted on the data bus 22B. The address bus 22A may include the address of the block addressed by the transaction, a TID, and a command (CMD) indicating the transaction (e.g. one of the transactions shown in FIG. 8, for one embodiment). Additional address bus signals may be included as desired to indicate other attributes of the transaction. The data bus 22B may include the data for the transaction and the TID (used to match the data phase to the corresponding address phase). Additional data bus signals may be included as desired (e.g. error signals, etc.). The interconnect 22 may include response (RSP) lines 22C on which the memory bridge 32 is configured to provide a response (and response lines on which other coherent agents are configured to provide a response, not shown in FIG. 3) during the response phase of the transaction. The interconnect 22 may further include an F_TID bus 22D on which the memory bridge 32 may transmit the TID of a pended transaction to the data source of the transaction, to indicate that the data may be transferred." (Emphasis added)

Rowlands 1 also illustrates in the timing diagram of FIG. 7, and teaches at col. 17. lines 33-65

"Turning next to FIG. 7, a timing diagram is shown illustrating one embodiment of a RdExc transaction to a block A. Time increases from left to right in FIG. 7.

An agent initiates the transaction on the address bus 22A, assigning a TID

> of 10 to the transaction. Subsequently, the response phase for the transaction occurs. The response from the memory bridge 32 is shared on the RSP lines 22C, indicating that the data is to be pended. The memory controller 14 (the data source for this transaction) detects the pended data case due to the memory bridge 32's shared response. The response phase may occur at any point after the address phase of the transaction, in various embodiments. The response phase may be a fixed or programmable time period after the address phase. In one embodiment, the response phase may be fixed at two bus clock cycles after the address phase.
>
> ....
>
> A similar timing diagram may be applicable to a WrInv transaction, except that the same agent may source the address and the data of the transaction; Additionally, a response from the memory bridge 32 of either shared or exclusive may cause a data pend for the WrInv transaction." (Emphasis added)

From the above disclosure as wel as others in Rowlands, it is clear that interconnect 22 is a bus system for conveying bus transactions and not packets. rowlnads is clear in other sections where packets are received by, for example te packet DMA 16, and trasactions are sent on interconnect 22. Accordingly, Applicant submits Rowlands1 does not teach or disclose "an address network configured to convey address packets between the interface and the plurality of active devices, and a data network configured to convey data packets between the interface and the plurality of active devices, wherein the address network and the data network are separate networks," as recited in claim 7.

The Examiner also asserts Rowlands teaches sendfing proxy address packets (probe commands). Applicant respectfully disagrees with the examiner's characterization that a probew command is the same as a proxy address packet. Typically, a probe command gets sent by a requesting processor to all other entities in a system. Not so with a proxy address packet. The proxy address packet is sent within a node by the interface of that node in response to receiving a coherency message requesting a read access right to a coherency unit from another node's interface. This is clearly different and recited in claim 7.

Thus Applicant submits none of the cited references teach or suggest "a node including a plurality of active devices and an interface coupled by an address network configured to convey address packets between the interface and the plurality of active devices, and a data network configured to convey data packets between the interface and the plurality of active devices, wherein the address network and the data network are separate networks," or "wherein the interface is configured to respond to the coherency message by sending a proxy address packet on the address network," as recited in claim 7.

For the foregoing reasons, Applicant submits claim 7, along with its dependent claims patentably distinguishes over the cited references.

Claims 18, and 22 recite features that are similar to features recited in claim 7. Accordingly, Applicant submits claims 18 and 22, along with their respective dependent claims patentably distinguish over the cited references for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-25901/SJC.

Respectfully submitted,

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